REMARKS

This AMENDMENT UNDER 37 CFR 1.111 is filed in reply to the outstanding Office Action of July 14, 2004, and is believed to be fully responsive thereto for reasons set forth below in greater detail.

Responsive to the objection to the drawings, Replacement Sheets for Figures 1-3 and 5 are submitted herewith.

Reconsideration is respectfully requested of the rejection of:

claims 1, 2, and 8 under 35 U.S.C. 102(b) as being anticipated by Kudoh; and

claims 3-7 and 9 under 35 U.S.C. 103(a) as being unpatentable over Kudoh in view of Applicants' prior art figure 1.

The present invention provides dense SRAM cells fabricated with selective SOI (SSOI) that involves the selective placement of buried oxide only in the areas where it is needed, as opposed to blanket SOI that provides SOI everywhere across the chip. A SRAM cell fabricated in SSOI comprises cross coupled PFET pull-up devices P1, P2 and NFET pull-down devices N1, N2, with the P1, P2 devices being connected to the power supply and the N1, N2 devices being connected to the ground. A first passgate NL is coupled between a first bitline and the junction of the devices P1 and N1, with its gate coupled to a wordline, and a second passgate NR is coupled between a second bitline and the junction of devices P2 and N2, with its gate coupled to the wordline. Each of the pull-up devices P1, P2, the pull-down devices N1, N2, and the first and second passgates NL, NR are fabricated with selective SOI, with buried oxide being selectively provided under the drains of the pull-up devices P1 and P2, the drains of the pull-down devices N1 and N2, and the sources and drains of the passgate devices NL and NR.

Both the pull-up devices P1 and P2 and the pull-down devices N1 and N2 are provided with selective SOI under the drain D regions as the SOI reduces the capacitance of the drain D to allow the potential on the drain D to be moved/changed faster to increase the circuit speed. The sources S of the pull-up devices P1 and P2 are biased/coupled to VDD, while the

AMENDMENTS TO THE DRAWINGS

The amendments to Figures 1-3 and 5 in the Replacement Sheets submitted herewith merely add the label "PRIOR ART" to each of Figures 1-3 and 5.

sources S of the pull-down devices P1 and P2 are biased/coupled to ground GND, and so the potential of the sources S does not move/change, and so a lesser capacitance is not required. Moreover, a greater capacitance at the sources S aids the stability of the SRAM cell, and so selective SOI is not provided under the sources S of both the pull-up devices P1 and P2 and the pull-down devices N1 and N2. The channels under the gates G of the pull-up devices P1 and P2 should be biased/touched to VDD of the underlying N well, and the channel under the gates G of the pull-down devices N1 and N2 should be biased/touched to GND of the underlying P well, and so selective SOI is also not provided under the gates G of both the pull-up devices P1 and P2 and the pull-down devices N1 and N2.

The explanation of Kudoh in the prior art rejection states,

"Kudoh discloses an SRAM cell fabricated in selective silicon on insulator comprising cross coupled pnp pull-up devices (QT11 and QT12), npn pull-down devices (QM11 and QM12), and passgates (QM13 and QM14). Note figures 11A and 11C of Kudoh. Figures 9, 10, and 11C clearly show that the pull-up devices, the pull-down devices, and passgates are selectively provided with SOI or being fabricated over bulk silicon without SOI."

These statements represent an incomplete explanation of Kudoh.

In summary, in Kudoh, the NFETs are fabricated over bulk silicon with no oxide at all, and the PFETs are fabricated with a blanket oxide coating under all of the components of the PFETs.

In summary, Kudoh does not provide selective oxide isolation similar to the present invention. Kudoh discloses an optimized layout for a TFT (Thin Film Transistor), and the oxide on the PFET TFT is present under all components of the PFET TFT whether it is needed or not.

The pullup devices (QT11 & QT12 of Fig. 11) are TFT (Thin-Film-Transistor) devices over blanket oxide. The source/drain has the advantage of lighter capacitance, but has an undesirable floating voltage body. It is somewhat like CMOS technology on blanket oxide.

In contrast to Kudoh, in the present invention, Fig. 4, the pullup devices only have oxide under the drain. No oxide is provided under the gate to allow for body contacts. Body contacts are needed to prevent the problematic floating voltage body effects. No oxide is provided under the VDD source to provide the supply stabilization.

The NFETs of the Kudoh patent are conventional NFET devices over bulk silicon without any oxide isolation. As explained in the present patent application, bulk silicon devices are slower even though the body can be biased. In the Kudoh patent, there is no oxide isolation at all for the NFETs QM11, QM12, QM13, QM14. (Fig. 11)

In the present invention, the selective oxide is provided only under the moving voltage nodes. Again, no oxide is provided under the gates for body contacts, and no oxide is provided under the pulldown NFET source for GND stabilization.

The Kudoh patent concerns a TFT (Thin Film Transistor) wherein the TFT device body, source and drain are polysilicon instead of monocrystalline silicon. Below the TFT PFET device body, source and drain is a blanket oxide insulation. In a way it is like conventional 'SOI' CMOS technology where the insulator is a blanket of silicon dioxide.

Thus in 'SOI' silicon CMOS technology, the oxide is present under the device body, source and drain. In the 'bulk' silicon CMOS technology, no oxide is present under the device body, source or drain.

It is black or white and there are no other choice. The Kudoh patent is all black, with oxide under all of the source and drain in the PFET TFT, and all white, with no oxide under all of the source and drain in the NFET TFT.

Claim 1 (Amended) clearly distinguishes over Kudoh by specifying that the drains of the pull down devices N1 and N2 are provided with selective SOI, as the NFETs in Kudoh are fabricated over bulk silicon with no oxide at all.

This application is now believed to be in condition for allowance, a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might

expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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